REMARKS

Claims 14, 15, 17 to 26, and 28 to 30 are currently pending in the present application.

In view of this response, it is respectfully submitted that all of the presently pending claims are allowable, and reconsideration is respectfully requested.

With respect to paragraph ten (10) of the Final Office Action, claims 14, 15, and 17 to 26 were rejected under 35 U.S.C. § 103(a) as unpatentable over Mason et al., "A Generic Multielement Microsystem for Portable Wireless Applications" (the "Mason" reference), in view of U.S. Patent Application Publication No. 2002/0194548 (the "Tetreault" reference).

To reject a claim under 35 U.S.C. § 103(a), the Office bears the initial burden of presenting a *prima facie* case of obviousness. *In re Rijckaert*, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). To establish *prima facie* obviousness, three criteria must be satisfied. First, there must be some suggestion or motivation to modify or combine reference teachings. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). This teaching or suggestion to make the claimed combination must be found in the prior art and not based on the application disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991).

Also, as clearly indicated by the Supreme Court in *KSR*, it is "important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the [prior art] elements" in the manner claimed. *See KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727 (2007). In this regard, the Supreme Court further noted that "rejections on obviousness cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *Id.*, at 1396. Second, there must be a reasonable expectation of success. *In re Merck & Co., Inc.*, 800 F.2d 1091, 231 U.S.P.Q. 375 (Fed. Cir. 1986). Third, the prior art reference(s) must teach or suggest all of the claim features. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974).

Claim 14 relates to a control unit, including a housing, a processor, and at least one inertial sensor, in which a data transmission between the processor and the at least one inertial sensor is digital, and in which *the data transmission is configured in such a way that transmitted data has at least one error bit and at least one status bit, the at least one error bit enabling detection and identification of data transmission errors*, and *the at least one status bit enabling recognition of an operating state of the at least one inertial sensor.*

The "Mason" reference does not disclose (or even suggest) all of the features of claim 14. Indeed, the prior Office Action of August 13, 2007 admitted at page 4 that the "Mason" reference does not "specifically teach[] the data transmission is configured in such a way that transmitted data has at least one error bit and at least one status bit." Nonetheless, the Final Office Action conclusorily asserts that "it is clear that the data transfer between sensor and processor has some signal or bit in a signal or pulse in a signal waveform to send/receive information about the above valid or invalid data and the state or mode of operation." (Final Office Action, pp. 4 to 5). In fact, the "Mason" reference does not disclose that the transmitted data includes at least one error bit and at least one status bit. Instead, the "Mason" reference merely indicates that its data format includes a 4-b chip address, a 3-b command, and a 5-b element address. (Mason, p. 1737, col. 1, lines 31 to 40). Further, Figure 5 of the "Mason" reference merely shows a DV (Data Valid) bus line that is separate from the transmitted data format. (Mason, p. 1737, col. 2, lines 4 to 8). Therefore, the transmitted data of the "Mason" reference does not have "some signal or bit in a signal or pulse in a signal waveform to send/receive information about the above valid or invalid data and the state or mode of operation," as asserted by the Final Office Action.

Thus, the "Mason" reference plainly does not disclose the feature of the *transmitted data has at least one error bit and at least one status bit*, as provided for in the context of claim 14. As a result, the "Mason" reference also cannot disclose the features of *the at least one error bit enabling detection and identification of data transmission errors*, and *the at least one status bit enabling recognition of an operating state of the at least one inertial sensor*, as provided for in the context of claim 14.

Still further, even if the "Tetreault" reference may refer to a bus interface logic 38 that generates a bus status signal (Tetreault, ¶¶ 19 and 38), and even if the "Tetreault" reference may indicate that a bank of device state registers 62 stores state information for devices 32 (Tetreault, ¶¶ 28, 29, and 38), the "Tetreault" reference simply does not disclose that the transmitted data includes at least one error bit and at least status bit. Instead, the bus status signal (STATUS) and the state information stored in the device state registers 62 of the "Tetreault" reference are independent and separate from any potentially transmitted data. In this regard, the bus status signal (STATUS) merely indicates whether the bus is idle or busy. (Tetreault, ¶ 19). Further, the error detectors 44, 46, 48 of the "Tetreault" reference merely generate a signal (ISOLATE) indicating a device to be isolated. (Tetreault, ¶ 31). However,

nowhere does the "Tetreault" reference disclose transmitted data that includes at least one error bit and at least one status bit.

Thus, the "Tetreault" reference plainly does not disclose the feature of the *transmitted data has at least one error bit and at least one status bit*, as provided for in the context of claim 14. As a result, the "Tetreault" reference also cannot disclose the features of *the at least one error bit enabling detection and identification of data transmission errors*, and *the at least one status bit enabling recognition of an operating state of the at least one inertial sensor*, as provided for in the context of claim 14. In this regard, none of the signals of the "Tetreault" reference provides for detection and identification of data transmission errors, or recognition of an operating state of the at least one inertial sensor. Instead, the "Tetreault" reference merely seeks to isolate identified devices from the bus by sending (ISOLATE) and (CONTROL) signals, without identifying the data transmission errors, or recognizing an operating state of the at least one inertial sensor.

Accordingly, it is respectfully submitted that claim 14 is allowable, since the "Tetreault" reference does not cure the critical deficiencies of the "Mason" reference.

Claims 15, and 17 to 26 depend from claim 14, and are therefore allowable for essentially the same reasons as claim 14.

Withdrawal of the rejections of the claims is therefore respectfully requested.

With respect to paragraph eleven (11) of the Final Office Action, claims 28 to 30 were rejected under 35 U.S.C. § 103(a) as unpatentable over the "Mason" reference, in view of the "Tetreault" reference, and further in view of U.S. Patent Application Publication No. 2002/0173930 (the "Perner" reference).

As explained above, the combination of the "Mason" reference and the "Tetreault" reference does not disclose (or even suggest) all of the features of claim 14. Claims 28 to 30 depend from claim 14, and are therefore allowable for essentially the same reasons provided above, since the "Perner" reference does not cure - and is not asserted to cure - the critical deficiencies of the combination of the "Mason" reference and the "Tetreault" reference.

Withdrawal of the rejections of the claims is therefore respectfully requested.

In sum, claims 14, 15, 17 to 26, and 28 to 30 are allowable.

CONCLUSION

It is therefore respectfully submitted that all of the presently pending claims are allowable. It is therefore respectfully requested that the rejections (and any objections) be withdrawn, since all issues raised have been addressed and obviated. An early and favorable action on the merits is therefore respectfully requested.

Respectfully submitted,
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